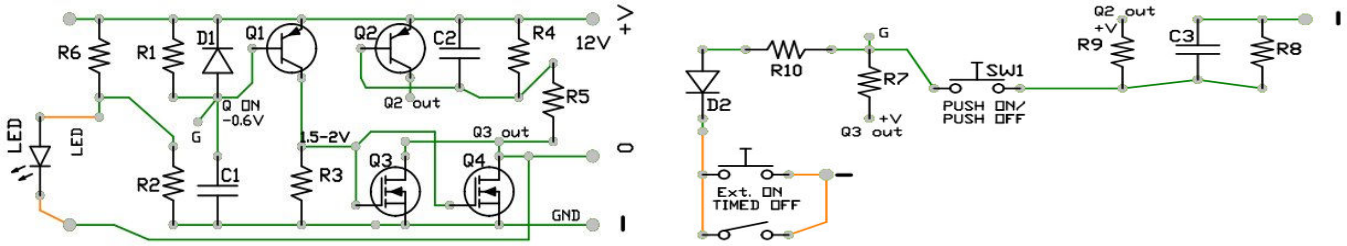
PEVDC Setup:

Schematic layout.



Parts List:
Standard latching ON/OFF switch.

Part	Type, Pattern	Note
Q1	PNP, SOT-23	ON/OFF gate control (Q3 output)
Q2	PNP, SOT-23	+/-V latch signal
Q3,Q4	N-CH, SOT-23	Output load switch
R1,R4,R5,R7,R8	Res, 0805	+/-V latch voltage delay
R2	Res, 0805	Dummy load
R3	Res, 0805	Q1 load
R9	Res, 0805	+/-V latch voltage hold delay
R10	Res, 0805	Exernal ON switch limit
C1	Cap, 0805	Switch debounce
C2	Cap, 0805/Ele	+/-V latch delay time
C3	Cap, 0805	+/-V latch voltage hold
LED	LED, axial	Output signal
SW1	SW, SMD	4.5/6mm tactile switch
SW Ext.	Switch	Exernal ON switch
D1,D2	Diode, SOD-323	Signal diode

Setup 1:
12V ON/OFF Basic setup. Latching switch.

Part	Value
Q1,Q2	2N3906, generic PNP
Q3,Q4	N-CH, SOT-23, >2.0Vgs, power switch
R1,R4,R5,R7,R8	1.0M (750k-1.2M) resistor
R3	10k (4.7-15k) load
R9	27-33k, R8/R9 Vdivider 0.3-0.5V (Q1 base off)
C1	0.1uF (0.1-0.47uF, 104-474)
C2	33uF (10-47uF)
C3	1.0uF (105)

Q1 and Q2 can be P-CH MOSFETs. The Vgs trigger is not as consistent as PNP transistors. MOSFETs allow for longer time delay and higher resistor values.